# A GaAs MESFET Transient Model Capable of Predicting Trap-Induced Memory Effects Under Complex Digital Modulation

F. Wang*, W. D. Jemison*, J. C. M. Hwang**

*Department of ECE, Lafayette College, Easton, PA 18042 USA
**Department of E.E.C.S, Lehigh University, Bethlehem, PA 18015 USA

***Abstract* — A transient model for GaAs MESFETs is presented that can predict distortion of digitally modulated carrier waveforms due to memory effects induced by both low-frequency dispersion and gate-lag. Experimental and simulated results are presented which demonstrate, for the first time, the successful prediction of these effects for multi-level pulse modulated waveforms.**

## I. INTRODUCTION

There has been much work on the modeling of trap induced memory effects in GaAs MESFETs. Two important memory effects include low frequency dispersion of the device output resistance due to the steady state trapping equilibrium established at a given excitation as well as gate lag effects due the transient trapping dynamics [1,2,3].

Traditionally, these two effects have been treated separately. Recently, however, Leoni, et al. reported on a transient SPICE model for GaAs MESFETs that could simultaneously simulate both low frequency dispersion and gate-lag [4,5]. In this approach, a voltage-controlled variable resistance was added to the drain of a conventional (*e.g*. Curtice) MESFET model to account for low frequency output resistance dispersion. In addition, an anti-parallel voltage controlled current source was used to account for the effects of gate-lag due to the charging and discharging of surface and/or bulk traps. The controlling voltage for both the variable resistance and the controlled current source are derived from a set of non-linear RC sub-circuits that simulate both the charging and discharging of the traps. Several of these sub-circuits may be used to account for multiple types of traps.

These trap-induced memory effects can produce distortion of digitally modulated RF waveforms since the symbol duration may be commensurate with the trapping time constants (several seconds to tens of microseconds). Therefore, it is important for wireless design applications that models be developed that can accurately predict these effects. Moreover, it is important that these models be able to accommodate more complex digital modulation formats such as M-ary PSK. This is a challenging problem since the trapping effects are bias dependent and have memory and are thus dependent on the entire waveform history.

The experimental and simulated results presented by Leoni, et. al. focused on simple on-off pulse modulation. Only single transient events (*i.e.* either RF pulse-on or RF pulse-off) were presented. In order for this modeling approach to be generally applicable to modern wireless design, it must be modified to handle more complex digital modulation formats. Furthermore, it is desirable to use an envelope simulator rather than a pure time domain simulator such as SPICE such that high frequency carriers with low frequency modulation can be efficiently simulated and spectral effects can be more easily investigated.

In this paper, we present a GaAs MESFET transient model that includes a modified RC sub-circuit approach designed to allow the accurate simulation of complex digitally modulated RF waveforms. This model has been implemented in a commercially available envelope simulator and may, therefore, be used to simulate modulated RF and microwave carrier waveforms. Simulation and experimental results are presented for both a multi-level pulsed dc waveform and a multi-level pulsed low-frequency (40 kHz) carrier waveform. Pulse segment interactions due to trap induced memory effects are clearly evident and are accurately predicted.

## II. MODEL CONSTRUCTION

The general model topology is shown in Figure 1 and includes a standard high frequency MESFET model and a set of three RC sub-circuits to account for trap charging and discharging. The outputs of the RC sub-circuits are then used to control a variable drain resistance to model low frequency output resistance dispersion and a controlled current source to model gate lag.

0-7803-6540-2/01/$10.00 (C) 2001 IEEE

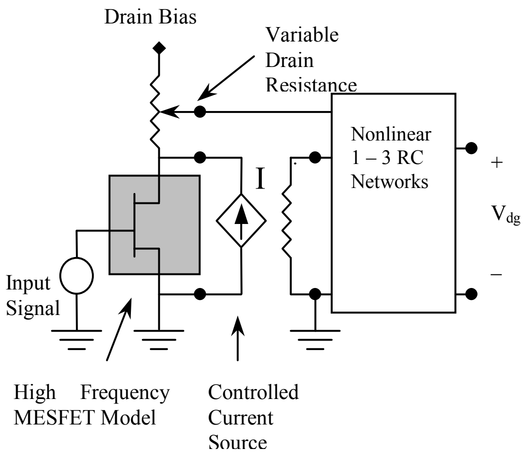


Fig. 1. Transient GaAs MESFET model topology

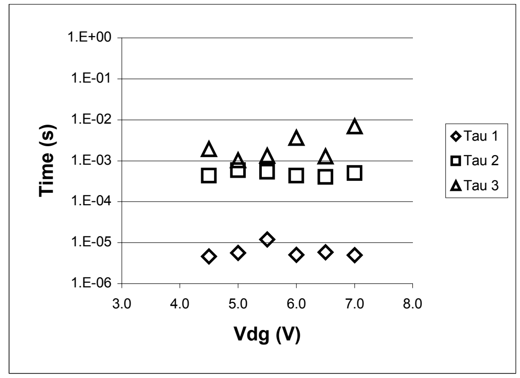


Fig 2b. Experimentally Extracted Discharging Time Constants

The specific model presented in this work was extracted from a GaAs MESET fabricated by vapor-phase epitaxy. The device has a gate length and width of 0.3 and 300 µm, respectively. The trapping charging and discharging time constants were extracted using a technique reported by Rippke, *et. al.* that uses the Nelder-Mead direct search method on pulsed waveform data taken at a number of different bias and pulsing conditions [6]. This efficient extraction technique yields three time constants and their associated amplitudes that characterize the trap charging behavior. These time constants in the range of several seconds to several hundred microseconds. The time constants are independent of the drain to gate voltage as shown in Figure 2.

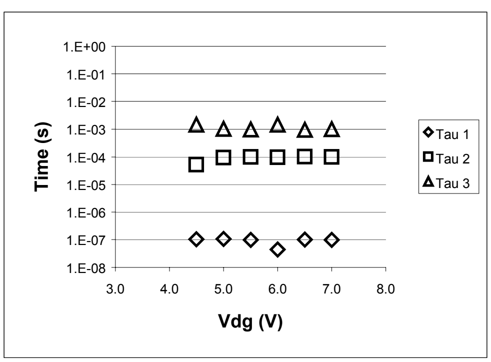


Fig 2a. Experimentally Extracted Charging Time Constants

As evident from the previous figures, the charging and discharging time constants are different. Furthermore, the amplitude weighting functions (not shown) for the charging and discharging time constants are also different. In order to successfully model complex waveforms, a non-linear RC sub-circuit must be used which provides independent control of the charging and discharging time constants and their amplitudes. The RC sub-circuit topology shown in Figure 3 has been developed to provide this function. The ideal diode provides the switching function between the charging and discharging time constants. Voltage controlled sources and summing junctions are then used to implement equation (1) to allow different amplitude weightings for the charging and discharging circuits to be implemented easily without introducing circuit loading effects.

$$I = \sum_{i=1}^{3} \left(Vc_i Ac_i + Vd_i Ad_i\right) / Rs \qquad (1)$$

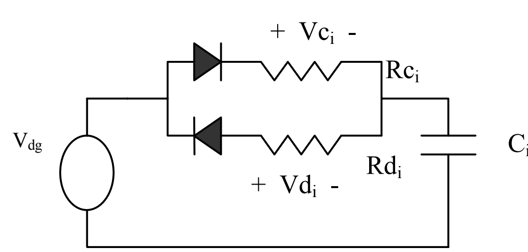


Fig. 3. Non-linear RC sub-circuit

The MESFET DC I-V curves were modeled in our present work using the following equation:

$$i_{ds} = i_{dsat} \cdot \tanh(\frac{v_{ds}}{v_{dsat}})(1+\lambda v_{ds}) \quad (2)$$

$$i_{dsat} = \frac{\beta(v_{gs} - VT)^n}{1 + b(v_{gs} - VT)^m} \quad (3)$$

Alternatively, a conventional MESFET model could also be utilized. The measured and modeled DC I-V characteristics are shown in Figure 4.

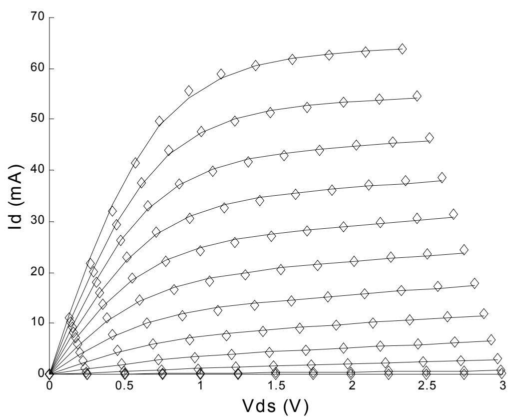


Fig. 4. Measured (◊) and Simulated (—) DC I-V curves.

## II. EXERIMENTAL VERIFICATION

In order to verify the accuracy of the model two waveforms were created using an arbitrary waveform generator. The waveforms were applied to the gate of the MESFET and the drain current was calculated using the voltage waveform measured across a 10 Ω drain resistor as shown in Figure 5.

The first waveform used for verifications is a multi-level dc (i.e. no carrier) pulse waveform. The simulated and measured waveforms are shown in Figure 6. The accuracy is within +/- 1 mA and the results clearly show that the model is able to predict the interaction of various pulses.

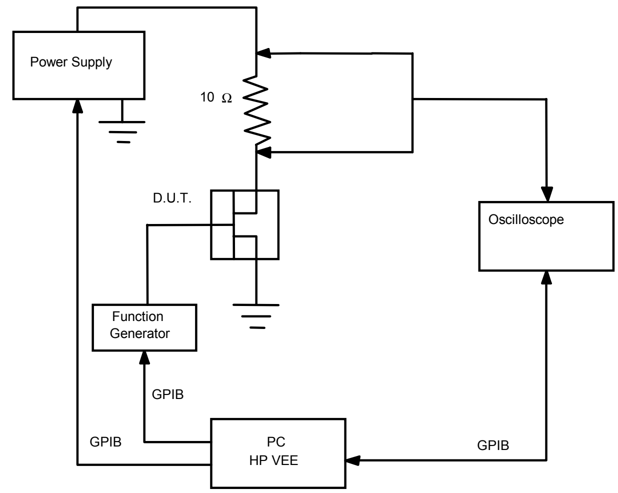


Fig. 5. Measurement set-up

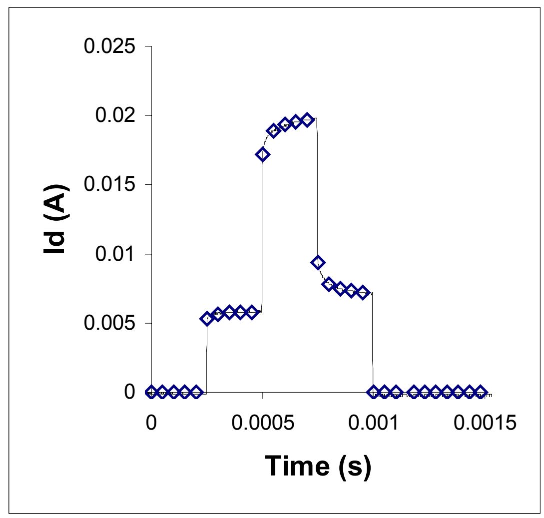


Fig. 6. Measured (◊) and simulated (—) waveforms for the multi-level dc pulse.

The second waveform used for verification is a multi-level pulse waveform with a low-frequency (40 kHz ) carrier. The selection of a low frequency carrier was based on available equipment that could generate arbitrary waveforms. The simulated and measured waveforms are shown in Figure 7. The accuracy is also within +/- 1 mA. It should be noted, that the trap induced transient effect may be small. However, small effects are important in accurately predicting low-level distortion measures such as ACPR.

The previous two results are illustrative of the accuracy that has been achieved using other drain bias and waveform variations. Also, it is important to note that there is nothing inherent in the modeling approach that precludes going to higher RF or microwave carrier frequencies.

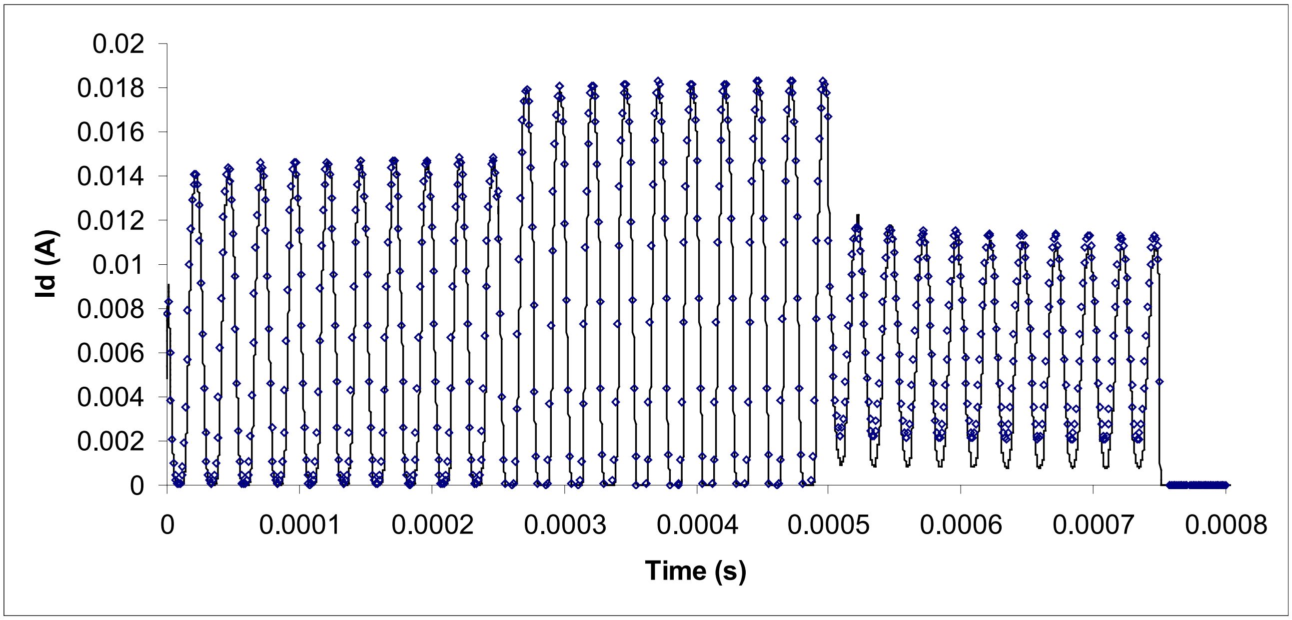


Fig. 7. Measured (◊) and simulated (—) waveforms to the multi-level pulsed carrier waveform.

## III. CONCLUSIONS

A transient GaAs MESFET model is presented which can predict trap-induced memory effects when the device is excited by complex digitally modulated waveforms. This was accomplished by developing a new RC sub-circuit to provide independent control of the charging and discharging time constants and amplitudes. The model was implemented in a commercially available envelope circuit simulator and was verified experimentally using multi-level pulsed dc and low-frequency carrier waveforms. This is the first time that trap-induced memory effects have been successfully simulated using a modulated waveform similar in complexity to modern wireless waveforms. The approach presented here does not have the limitations of previously reported SPICE implementations and can, therefore, be used with higher RF or microwave carrier frequencies.

## ACKNOWLEDGEMENT

This work was supported by NSF grant #ECS-9900085. The authors also acknowledge the support of the Lafayette College EXCEL scholars program.

## REFERENCES

[1] F. Filicori, G. Vannini, A. Santarelli, A. Sanchez, A. Tazon, and Y. Newport, "Empirical modeling of low-frequency dispersive effects due to traps and thermal phenomena," *IEEE Trans. Microwave Theory and Techniques,* vol. 43., pp 2972-2981, Dec. 1995

[2] J. Golio, M. Miller G. Maracas, and D. Johnson, "Frequency-dependent electrical characteristics of GaAs MESFET's," *IEEE Trans. Electron Dev.*, vol. 37, pp. 1217-1227, May 1990.

[3] D. Siriex, D. Barataud, R. Sommet, O. Noblanc, Ch. Brylinski, J. P. Teyssier, and R. Quere, "Characterization and modeling of nonlinear trapping effects in power SiC MESFETs," *2000 IEEE MTT-S Int. Microwave Symp. Dig.*, CD-ROM, June 2000.

[4] R. E. Leoni III, J. M. Bao, M. S. Shirokov, and J. C. M. Hwang, "A Physically-Based Transient SPICE Model for GaAs MESFET's," *1998 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 607-610, June 1998

[5] M. S. Shirokov, R. E. Leoni III, J. M. Bao, and J. C. M. Hwang, "A Physically-Based Transient SPICE Model for Digitally-Modulated RF Characteristics of Ion-Implanted GaAs MESFET's," *IEEE Trans. Electron Dev.*, pp. 1680-1681, Aug. 2000.

[6] I. A. Rippke, F. Wang, W. D. Jemison, M. S. Shirokov, and J. C. M. Hwang, "An Improved Low Frequency Transient Model Extraction Procedure for GaAs MESFET's," *IEEE Sarnoff Symposium. Dig*, March 2000.